OPTIMIZATION OF TRADE-OFFS BETWEEN EFFICIENCY AND INTERMODULATION IN SSPAs BASED ON EXPERIMENTAL AND THEORETICAL CONSIDERATIONS

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ABSTRACT

This paper examines the problem of improving trade-offs between power added efficiency and third order intermodulation in power FETs. Intermodulation and power added efficiency of a commercially available 4 watt power FET (FUJITSU FLM 7785-4C) have been fully characterized by using an active load pull technique. Significant variations of power added efficiency, third order intermodulation and differential gain compression versus bias conditions and load impedances are observed by experimentation and confirmed by theoretical non-linear analysis. Both experimentation and theoretical analysis proposed in this paper provide a valuable contribution to the optimization of trade-offs between power added efficiency and third order intermodulation in communication power amplifiers.

INTRODUCTION

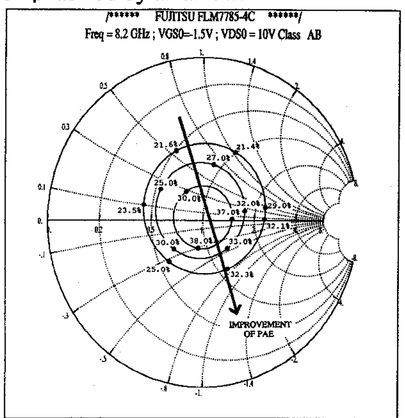
Improving trade-offs between power added efficiency and third order intermodulation in modern communication power amplifiers requires constant cares. Generally speaking, communication power amplifiers are designed and optimized to yield their maximum added power or power added efficiency. Then, for multitone applications, a sufficient back-off of the input power is specified not to exceed a given third order intermodulation ratio. This cannot be considered as a real optimization of trade-offs between power added efficiency (PAE) and third order intermodulation (IM3). An attractive method allowing to achieve this task is proposed in this paper. It consists in finding load dependance of both PAE and IM3 at any fixed input power of interest by computing power transistor load-pull measurements. A commercially available 4 Watt power FET (Fujitsu FLM 7785-4C) was fully characterized at 8.2 Ghz by using an active load-pull technique. It was found to be optimized in terms of power added efficiency under class AB operation. Appropriate computations of the large signal measurement data files show significant gradients of PAE and IM3 versus load. Such informations provide the right direction in which optimum trade-offs between these two features can be reached. The main results experimentally observed are verified and confirmed by a theoretical non-linear analysis based on non-linear electrical models of FET. Results of investigations concerning added power, third order intermodulation, load-lines and differential gain compression are reported.

I - ANALYSIS OF LOAD-PULL MEASUREMENT RESULTS OF A 4 WATT POWER FET

We designed and built a fully automated active load-pull system [1]. At the present time, this load-pull system covers the 1 - 18 GHz frequency bandwidth and allows the characterization of up to 10 watts CW power transistors. This system is fully error corrected for reflection and transmission coefficients. An exhaustive data-file of error corrected complex power waves at the fundamental operating frequency (a_1, b_1, a_2, b_2) is built for each component under test. Data files are then processed to compute the main characteristics of the device (complex gain, added power, power added efficiency, ...). In order to illustrate the capabilities of the system, we report measurement results of a 4 Watt power FET (Fujitsu FLM 7785-4C). This component was fully characterized at 8.2 Ghz with the aim of designing an optimized power amplifier for a satellite beacon application.

I.1 - Power added efficiency

Figure 1 shows the load dependence of power added efficiency. Under class AB bias conditions, constant added power contours are drawn on the Smith chart. Power added efficiencies are marked on the loci. A significant gradient of PAE is observed on any constant output power locus. This gradient is emphasized by an arrow.



P_{in} = 300 mW ; P_{add} = 2000, 2500, 3000 mW

Figure 1

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I.2 - Third order intermodulation

The design of multicarrier communication power amplifiers requires also an analysis of third order intermodulation (IM3). Assuming the narrow bandwidth approximation, IM3 can be predicted by computing the non-linear complex gain (single tone measurements). In our single tone measurement environment, the complex transmission coefficient b_2/a_1 of the device is accurately determined. This parameter takes into account combined effects of AM/AM and AM/PM conversions. For any fixed load impedance of interest, the non-linear function $b_2 = f_{NL}(a_1)$ is extracted from the measurement data file and fitted by a first order Bessel serie expansion [2].

$$b_2 = \sum_{k=1}^{\infty} \alpha_k J_1\left(\frac{\lambda_k a_1}{2 a_{1max}}\right) \qquad (1)$$

where : λ_k are the roots of $J_1(x)$

and α_k the complex coefficients of the serie.

Applying now the non-linear complex transform formalism, the response of the device to two same level input carriers can be predicted. Mathematical calculations lead to the following expression of the third order intermodulation ratio C/I :

$$10\log\left(\frac{C}{I}\right) = 10\log\left[\frac{\sum_{k=1}^{\infty} \alpha_k J_2\left(\frac{\lambda_k a_1}{2 a_{1max}}\right) J_1\left(\frac{\lambda_k a_1}{2 a_{1max}}\right)}{\sum_{k=1}^{\infty} \alpha_k J_1\left(\frac{\lambda_k a_1}{2 a_{1max}}\right) J_0\left(\frac{\lambda_k a_1}{2 a_{1max}}\right)}\right] \qquad (2)$$

C/I computations are achieved for different load impedances uniformely distributed on the constant added power contours of figure 1. Figure 2 shows both gradients of C/I and PAE versus load impedances. Under class AB operation, good trade-offs between PAE and C/I can be reached in accordance with user's specifications.

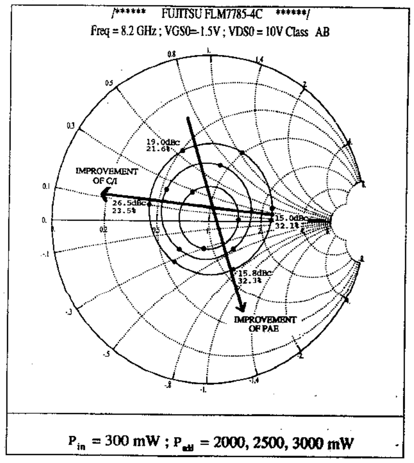

Figure 2

The differential gain compression (DGP) is another criteria providing valuable informations on non-linear devices .

The DGP is defined as follows :

$$DGP = \frac{G_{IS}}{\left.\frac{\partial P_{out}}{\partial P_{in}}\right|_{P_{in} = P_{in_o}}}$$

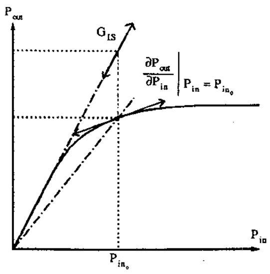

Figure 3

where G_{IS} is the low signal power gain.

By computing the first derivative of the complex non-linear gain, DGP can be determined for any fixed input power and load impedance of interest. Figure 4 illustrates the load dependence of both C/I and DGP at a fixed input power of 300 mW. Negative values of DGP indicates a weak gain expansion. It is also clearly observed that the variations of the differential gain compression are closely related to IM3 variations. The great interest of DGP lies in that it can be quickly and accurately determined by single tone measurements.

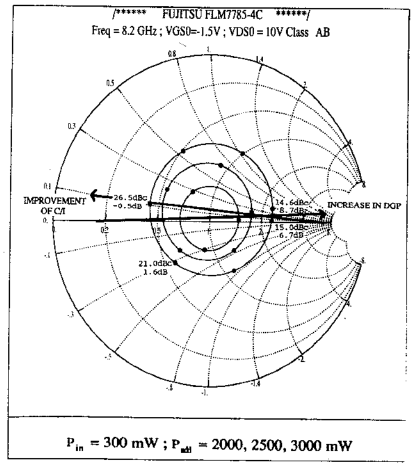

Figure 4

II - THEORETICAL ANALYSIS OF PAE, IM3 AND DGP IN POWER FETS

Theoretical analysis based on non-linear electrical models of FET are proposed. These theoretical analysis and the above experimental characterization are not performed by using the same FETs. Nethertheless, the aim of these analysis is to provide qualitative explanation and confirmation of experimental observations.

II.1 - Analysis of load dependence of both PAE and IM3.

At first, we propose a theoretical analysis based on a simplified drain current generator model described by equation 4. (Gopinath model).

$$I_{DS}(t) = I_{DSS}\left(1 + \frac{V_{GS}(t)}{Vp}\right)^2 \left(1 + \frac{V_{DS}(t)}{Ro\, I_{DSS}}\right) \qquad (4)$$

This equation is only valid in the saturation region of the I - V curves of the device :

That means : $V_{DSMIN} < V_{DS} < V_{DSMAX}$ (5)
(see figure 6)

This analysis is completed under class A operation :

$$V_{GSO} = \frac{V_\phi - Vp}{2} \; ; \; V_{DSO} = \frac{V_{DSMAX} + V_{DSMIN}}{2} \qquad (6)$$

- **Constant output power contours :**

Let us consider the following excitation voltages :

$$V_{GS}(t) = V_{GSO} + V_{GS1}\cos\omega t \qquad (7)$$

$$V_{DS}(t) = V_{DSO} - V_{DS1}\cos(\omega t + \varphi) \qquad (8)$$

(harmonic voltages terminated in short circuits).

Mathematical calculations of equations (4), (7) and (8) lead to constant output power contours (figure 5).

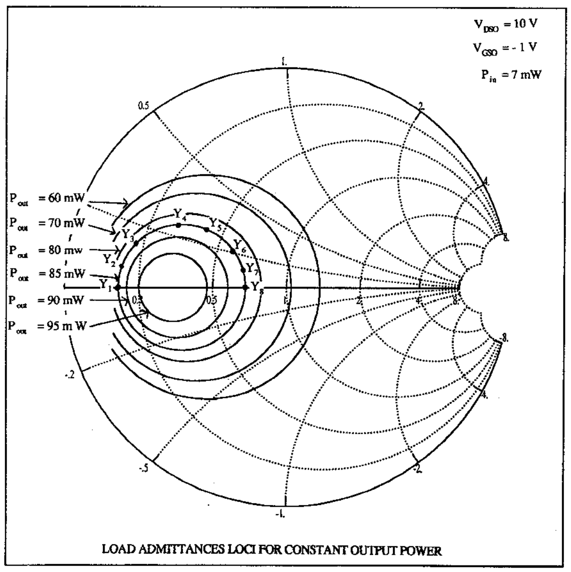

Figure 5

Contours associated to the lowest output power values are not fully closed because of the limitations of the model. In fact, condition (5) is not checked in these particular cases.

- **Load-lines**

Let us consider now admittances distributed on the 85 mW output power locus. (Y_1, Y_2, ..., Y_8 in figure 5). Load-lines associated to these admittances are drawn in the I.V. plane of the transistor (figure 6). All the load lines are tangent to the static characteristics $V_{GS} = V_{GSO} + V_{GS1}$ and $V_{GS} = V_{GSO} - V_{GS1}$. It indicates that the input power is kept constant. Load lines C_1 and C_8 have no area and are obtained with purely resistive admittances Y_1 and Y_8. These load lines are obtained at constant input and output powers.

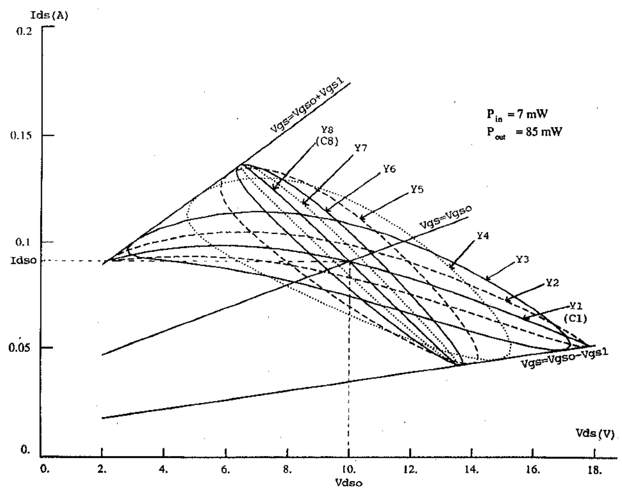

Figure 6

- **Power added efficiency and third order intermodulation**

°The analysis of load dependence of PAE shows that the improvement of PAE is associated to an increase in V_{DS1}. At fixed input and output powers, the best PAE is reached for the smallest value of Y_{LOAD} (maximum swing of V_{DS}) in the drain current generator plane.

° The third order intermodulation ratio C/I is analyzed by writing $V_{GS}(t)$ in equation 4 as the sum of two sinusoïdal signals with equal amplitude V_{GS1} but different frequencies. The resulting drain voltage includes third order intermodulation components. The load impedance is assumed to be constant at each frequency of interest (f_1, f_2, $2f_1 - f_2$, $2f_2 - f_1$). (narrowband approximation). The C/I ratio is computed for the same output load admittances than those used in the previous analysis of PAE. For constant input power, it is observed that the improvement of C/I is associated to a decrease in V_{DS1}. At fixed input and output powers, the best C/I is reached for the largest value of Y_{LOAD} (minimum swing of V_{DS1}) in the drain current generator plane. Under class A operation and at fixed input and output powers, the improvement of C/I is incompatible with the improvement of PAE. The best C/I is obtained for a minimum swing of V_{DS} while the best PAE is reached for a maximum swing of V_{DS}.

By superimposing loadlines, constant output power hyperbolas [3] and I.V curves, the graphical representation of figure 7 is obtained. The load-line C8 (V_{DS1MIN}) yields the best C/I ratio while the best PAE is obtained with the load line C1 (V_{DS1MAX}). Such a plot reveals to be a valuable graphical method to determine the optimum load admittance yielding the best value of power added efficiency or third order intermodulation at any fixed output power of interest.

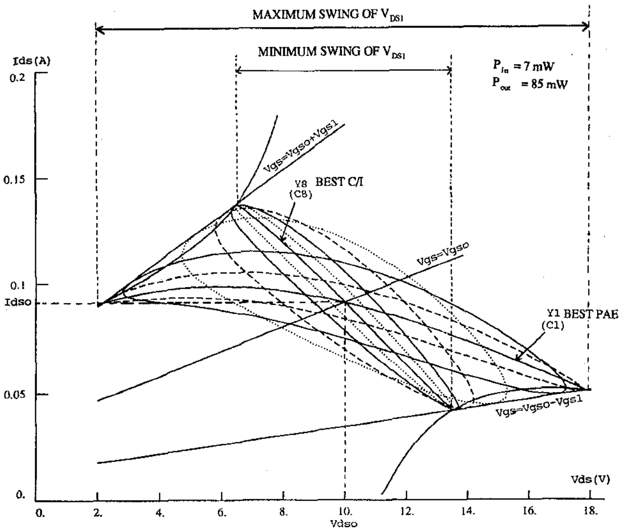

Figure 7

II.2 - Relation between C/I and DGP [4], [5]

A second theoretical analysis based on a classical non-linear FET model with four non-linearities is proposed. The drain current generator is decribed by Tajima equation (10 parameters). Simulations are performed with two same level input signals at different frequencies (Libra software). The whole input power is kept constant $(P_{in} = 12{,}5\ mW)$. The C/I ratio is computed for different purely resistive loads (Z_L) in the drain current generator plane.

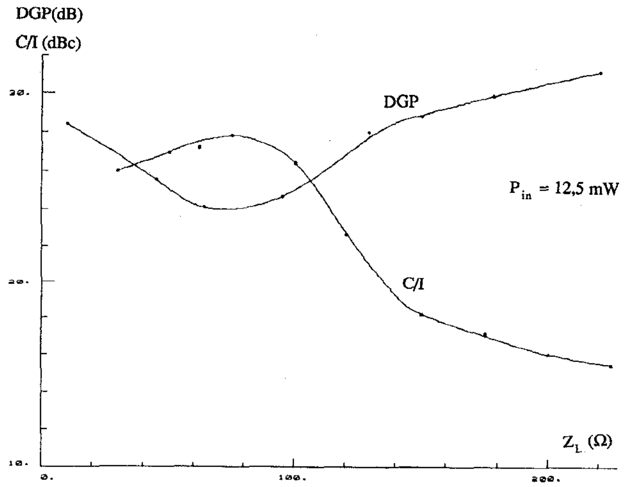

Figure 8

For the same load conditions, the differential gain compression (DGP) is calculated for a single tone 12,5 mW input signal. Variations of C/I and DGP versus Z_L are given in figure 8. It is clearly observed that the maximum value of C/I corresponds to the minimum value of DGP confirming so observations made by experimentations.

CONCLUSION

The analysis of a 4 watt power FET load-pull measurements shows significant gradients of PAE and IM3 versus load impedances. It allows an experimental optimization of trade-offs between IM3 and PAE in communication power amplifiers. Moreover, analytical calculations confirme observations made by measurements. The proposed analysis of load lines in the I-V plane of the FET provides a graphical method to optimize PAE or IM3 in power amplifiers. Numerical simulations achieved by using a Tajima model of FETs show a close relation between IM3 and DGP. The differential gain compression appears as an interesting parameter seeing that it can be easily determined by single tone measurements. As a conclusion, all these investigations provide a significant aid to the optimum design of solid state power amplifiers.

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